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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification ⁶: H01L 23/48, 23/52, 29/40	A1	(11) International Publication Number: WO 97/25742 (43) International Publication Date: 17 July 1997 (17.07.97)
(21) International Application Number: PCT/US96/20865 (22) International Filing Date: 30 December 1996 (30.12.96) (30) Priority Data: 08/581,021 3 January 1996 (03.01.96) US (71) Applicant (for all designated States except US): INTEL CORPORATION [US/US]; 2200 Mission College Boulevard, Santa Clara, CA 95052 (US). (72) Inventors; and (75) Inventors/Applicants (for US only): LODER, William, G. [US/US]; 3308 North Salida Del Sol, Chandler, AZ 85224 (US). McMAHON, John, Francis [US/US]; 4552 North Royal View Drive, Phoenix, AZ 85018 (US). (74) Agents: TAYLOR, Edwin, H. et al.; Blakely, Sokoloff, Taylor & Zafman, L.L.P., 7th floor, 12400 Wilshire Boulevard, Los Angeles, CA 90025 (US).		(81) Designated States: AL, AM, AT, AT (Utility model), AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, CZ (Utility model), DE, DE (Utility model), DK, DK (Utility model), EE, EE (Utility model), ES, FI, FI (Utility model), GB, GE, HU, IL, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SK (Utility model), TJ, TM, TR, TT, UA, UG, US, UZ, VN, ARIPO patent (KE, LS, MW, SD, SZ, UG), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, ML, MR, NE, SN, TD, TG). Published <i>With international search report.</i>
(54) Title: MULTI-CHIP INTEGRATED CIRCUIT PACKAGE <div data-bbox="349 1134 1299 1365" data-label="Image"> </div> (57) Abstract <p>An electronic package which has a plurality of stacked integrated circuit dies. The package includes a first die (12) that is mounted to a die paddle (16) of a lead frame (18). The first die is also connected to the leads of the lead frame by bond wires (28). A second die (14) is mounted to the top surface of the first die and electrically connected to the first die with bond wires. The first die, second die and die paddle are all enclosed by a package.</p>		

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MULTI-CHIP INTEGRATED CIRCUIT PACKAGE

BACKGROUND OF THE INVENTION

5 1. FIELD OF THE INVENTION

The present invention relates to a package for an integrated circuit.

10 2. DESCRIPTION OF RELATED ART

Integrated circuits (ICs) are typically housed within a package that is mounted to a printed circuit board assembly. The prior art includes a plastic package which is commonly referred to as a quad flat pack
15 (QFP). A QFP package typically contains a lead frame which has a plurality of leads that extend from an outer plastic package. The plastic encapsulates an integrated circuit that is coupled to the lead frame. The plastic package is typically produced by first mounting the integrated circuit onto a die paddle of the lead frame, and then interconnecting the
20 IC to the frame with a plurality of wire bonds. The integrated circuit and lead frame are then placed into a mold that is injected with a plastic dielectric material. The plastic material hardens and the assembly is removed from the mold. The lead frame is then trimmed and bent into a final configuration.

25 A final board assembly typically contains a number of integrated circuit packages mounted to a printed circuit board (PCB). The IC circuits communicate through the packages and the PCB. The inductance, capacitance and overall impedance of the packages and board are designed to minimize noise on the signals transmitted
30 between the integrated circuits. For high speed integrated circuits signal noise can be critical. To reduce noise, shorten trace lengths and the size of the printed circuit board, there have been utilized multichip

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modules (MCM) which can contain two or more integrated circuits. Multichip modules typically have a number of individual electronic devices mounted within the package in a laterally adjacent manner. The minimum footprint of a multichip module is limited by the outer dimensions of all the individual elements. Additionally, present multichip module substrates are typically constructed from ceramic, silicon, metal or printed circuit board materials which are relatively more expensive to produce than a plastic QFP. It would be desirable to provide an electronic package which has a minimal footprint and can be assembled with conventional plastic injection molding techniques without adding expensive interconnecting substrate components.

SUMMARY OF THE INVENTION

The present invention is an electronic package which has a plurality of stacked integrated circuit dies. The package includes a first die that is mounted to a die paddle of a lead frame. The first die is also connected to the leads of the lead frame by bond wires. A second die is mounted to the top surface of the first die and electrically connected to the first die with bond wires. The first die, second die and die paddle are all enclosed by a package.

BRIEF DESCRIPTION OF THE DRAWINGS

The objects and advantages of the present invention will become more readily apparent to those ordinarily skilled in the art after reviewing the following detailed description and accompanying drawings, wherein:

Figure 1 is a cross-sectional view of an electronic package of the present invention;

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Figure 2 is a top view showing a pair of integrated circuit dies and a lead frame;

Figure 3 is a cross-sectional view showing an alternate embodiment of the electronic package;

5 Figure 4 is a cross-sectional view showing an alternate embodiment of the electronic package;

Figure 5 is a cross-sectional view showing an alternate embodiment of an electronic package which has a plurality of discrete devices stacked in a pyramid arrangement.

10

DETAILED DESCRIPTION OF THE INVENTION

Referring to the drawings more particularly by reference numbers, Figure 1 shows an integrated circuit package 10 of the present invention. The package 10 contains a first die 12 and a second die 14. The first die 12 is mounted to a die paddle 16 of a lead frame 18. The first die 12 can be attached to the die paddle 16 by an epoxy, adhesive or any other suitable mounting material. The mounting material should preferably have a relatively high coefficient of thermal and/or electrical conductivity to improve the thermal and/or electrical efficiency of the package. The first die 12, second die 14 and die paddle 16 are encapsulated by a plastic to form a package 20. The lead frame 18 is typically constructed from an electrically conductive material such as copper alloy and contains a plurality of individual leads 22 that extend from the outer surface of the package 20. The package 10 is typically mounted to a printed circuit board (not shown) by soldering the ends of the leads 22 to corresponding pads of the printed circuit board. The leads 22 are typically bent into the gull-wing configuration shown. The stacked die arrangement reduces the overall length (footprint) of the package and size of the printed circuit board. The package of the present invention is therefore ideally suitable for products such as cellular phones or other relatively high density electronic devices.

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As shown in Figure 2, the second die 14 has a plurality of bonding pads 24 that are connected to a plurality of bonding pads 26 on the first die 12 by bond wires 28. The bonding pads 26 of the first die 12 are connected to the leads 22 of the lead frame 18 by bond wires 30.

5 Alternatively, all or some of the bonding pads 24 of the second die 16 may be bonded directly to the leads 22 of the lead frame 18.

Connecting the bonding pads 24 of the second die 14 to the bonding pads 26 of the first die 12 provides a direct bus between the two device without routing between the lead frame 22 or an external printed circuit board. The direct bus reduces the signal noise between the devices.

10 Additionally, the direct bus reduces the number of leads (pins) and the overall size of the package 10.

In the preferred embodiment, the first die 12 is a microprocessor and the second die 14 is a memory device. Alternatively, the second die

15 14 may be a memory device and the first die 12 may be an interposer. Referring to Fig. 2, the memory device 14 typically has bonding pads 24 located at two opposing ends of the die 14. The interposer 12 contains bonding pads 26 located along all four sides of the die 12. The bonding pads 26 of the interposer 12 are connected to corresponding leads 22 in

20 each quadrant of the lead frame 18. The four rows of bonding pads 26 on the interposer 12 "fan out" the interconnect from the two rows of second die bonding pads 24 to the lead frame 18. The interposer 12 therefore allows a conventional two row memory device to be attached to a conventional four row lead frame without having to redesign either

25 the device 14 or the lead frame 18.

Figure 3 shows an alternate embodiment of an electronic package 10' which has a heat slug 32 incorporated therein. The heat slug 32 extends through a hole in the package and is attached to the back side of the die paddle 16. The heat slug 32 extends from the die

30 paddle 16 to the outer surface of the package 20.

Figure 4 shows another alternate embodiment of a package 10" that has a heat slug 32 attached to the back side of the first die 12

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through a hole in the die paddle 16. The dies create heat that must be removed from the package. The heat transfer rate from the package must be sufficient to maintain the junction temperatures of the integrated circuits below a critical value. The heat slug 32 provides a thermal path
5 from the dies to the ambient that has a relatively low thermal resistance. The heat slug 32 therefore improves the overall thermal efficiency of the package. The heat slug 32 is preferably constructed from a material that is both thermally conductive and has a coefficient of thermal expansion that causes the overall package to match the thermal coefficient of the
10 printed circuit board on which the package is mounted.

Figure 5 shows another alternate package embodiment, wherein multiple dies 40a-c are stacked in a pyramid arrangement. Each upper die is mounted and electrically connected to an adjacent lower die by wire bonds. The lowest dies are then connected to the lead frame (not
15 shown) of the package. The "pyramid" stack of dies may be assembled within a package that has a heat sink 32, as shown in Figs. 3 and 4, or does not have a heat sink 32, as shown in Fig. 1. The top die 40b bridges two lower adjacent dies 40c. Although five dies are shown and described, it is to be understood that three or any number of dies may be
20 stacked in the arrangements shown and described.

The packages 10 of the present invention are preferably assembled by mounting the first die 12 onto the die paddle 16 and mounting the second die 14 onto the first die 12. The bonding pads of the dies are then connected to each other and the lead frame 18 by a
25 wire bonding process. Although the process is described as first mounting both dies to the die paddle and then wire bonding the device, it is to be understood that the order of steps may be altered. For example, the second die 14 may be mounted and wire bonded to the first die 12, before the first die 12 is mounted to the die paddle 16.

30 The lead frame and dies are placed into a mold (not shown). A plastic dielectric material is then injected into the mold cavity to create the outer package 20. If a heat slug 32 is to be incorporated into the

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package, the slug 32 can also be placed into the mold. Alternatively, the mold can be constructed to create a hole in the package, wherein the heat slug 32 is mounted into the hole after the plastic material has cured.

5 The package is removed from the mold after the plastic package has cured. The leads of the lead frame are then trimmed and bent into a final configuration. The present invention thus provides a multichip package that has a relatively small footprint and can be assembled using conventional plastic molding techniques.

10 While certain exemplary embodiments have been described and shown in the accompanying drawings, it is to be understood that such embodiments are merely illustrative of and not restrictive on the broad invention, and that this invention not be limited to the specific constructions and arrangements shown and described, since various
15 other modifications may occur to those ordinarily skilled in the art. Although a plastic package is shown and described, it is to be understood that the dies may be stacked within a ceramic package or metal based electronic package marketed under the trademark MQUAD.

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What is claimed is:

1. An electronic package, comprising:
a first die;
5 a second die mounted to said first die;
a package that encloses said first and second dies; and,
a conductive routing circuit that is located within said package
and is connected to said first and second dies.
- 10 2. The package as recited in claim 1, wherein said second die is
electrically connected to said first die.
3. The package as recited in claim 1, wherein said first die is a
memory device.
15
4. The package as recited in claim 3, wherein said second die is
a microprocessor.
5. The package as recited in claim 2, wherein said second die
20 has a plurality of bonding pads on a first end and a second end, and
said first die has a plurality of bonding pads on a first end, a second end,
a third end and a fourth end.
6. The package as recited in claim 1, wherein said conductive
25 routing circuit is a lead frame.
7. The package as recited in claim 6, wherein said first die is
mounted to a die paddle of said lead frame.
- 30 8. The package as recited in claim 7, further comprising a heat
slug attached to said die paddle.

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9. The package as recited in claim 7, further comprising a heat slug that extends through a hole in said die paddle and is attached to said first die.

5 10. The package as recited in claim 6, wherein said package is constructed from a plastic material.

11. The package as recited in claim 1, further comprising a third die mounted to said second die.

10

12. The package as recited in claim 1, wherein said conductive routing circuit is within a ceramic package.

13. An electronic package, comprising:
15 a lead frame that has a die paddle;
 a first die mounted to said die paddle;
 a second die mounted to said first die;
 a plurality of first wire bonds that connect said second die to said first die;
20 a plurality of second wire bonds that connect said first die to lead frame; and,
 a package that encloses said first die, said second die and said die paddle of said lead frame.

25 14. The package as recited in claim 13, wherein said first die is a memory device.

15. The package as recited in claim 14, wherein said second die is a microprocessor.

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16. The package as recited in claim 13, wherein said second die has a plurality of bonding pads on a first end and a second end, and said first die has a plurality of bonding pads on a first end, a second end, a third end and a fourth end.

5

17. The package as recited in claim 13, further comprising a heat slug attached to said die paddle.

18. The package as recited in claim 13, further comprising a heat slug that extends through a hole in said die paddle and is attached to said first die.

10

19. The package as recited in claim 13, further comprising a third die mounted to said second die.

15

20. An electronic package, comprising:

a first die;

a second die adjacent to said first die;

a third die that is mounted to said first die and said second die;

20 a package that encloses said first, second and third dies; and,
a conductive routing circuit that is located within said package and is connected to said first, second and third dies.

21. The package as recited in claim 20, wherein said third die is electrically connected to said first and second dies.

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22. A method for assembling an electronic package, comprising the steps of:

- a) mounting a first die onto a die paddle of a lead frame;
- b) mounting a second die onto the first die;
- 5 c) connecting the second die to the first die;
- d) connecting the first die to the lead frame; and,
- e) enclosing the first die, the second die and the die paddle of the lead frame within a package.

1 / 2

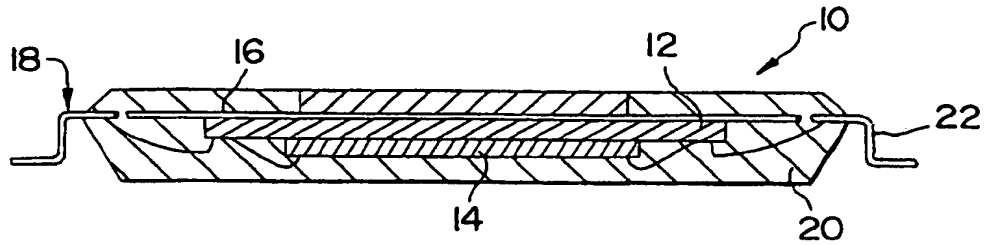


FIG. 1

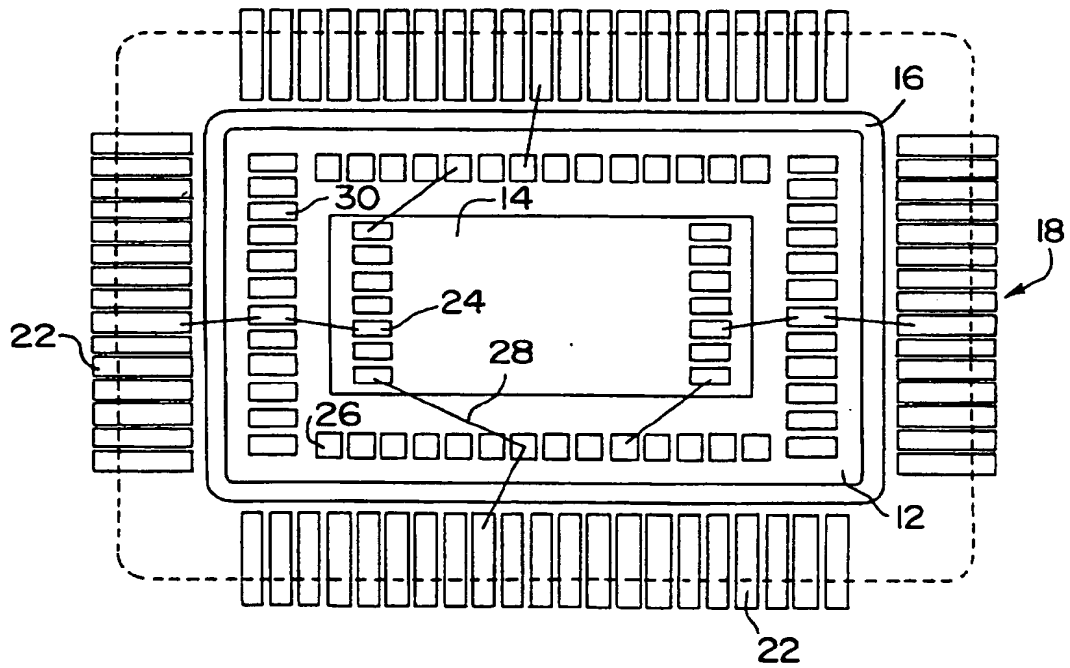


FIG. 2

2 / 2

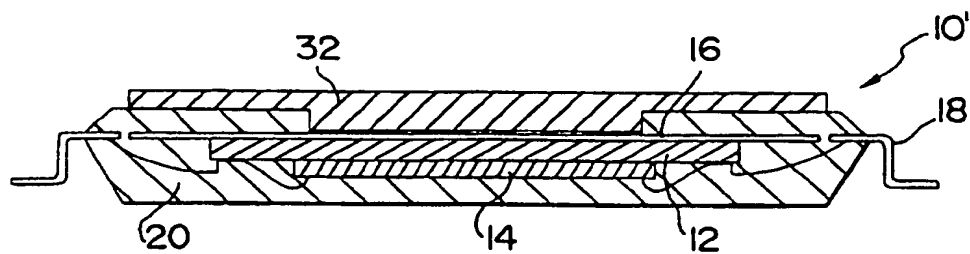


FIG. 3

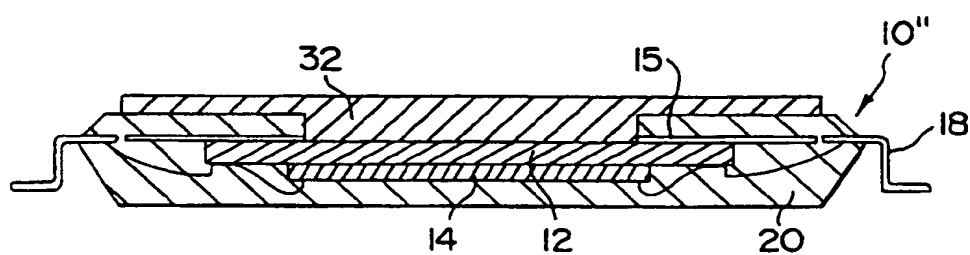


FIG. 4

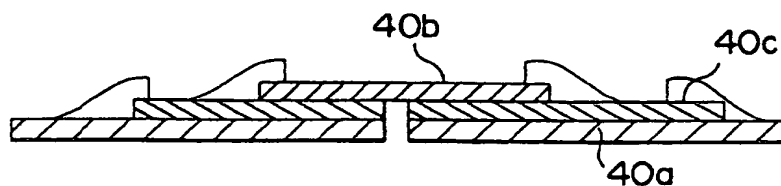


FIG. 5

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US96/20865**A. CLASSIFICATION OF SUBJECT MATTER**

IPC(6) : H01L 23/48, 23/52, 29/40

US CL : 257/777, 676

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 257/777, 676

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X ---	JP 3-165550 A (YASHIRO) 17 JULY 1991, FIGURE 1.	1-7, 13-16 -----
Y		8-12, 17-22
X ---	US 5,422,435 A (TAKIAR et al) 06 JUNE 1995, COL. 4, LINE 55 TO COL. 6, LINE 14.	20, 21 -----
Y		11, 19-22
Y	US 5,216,283 A (LIN) 01 JUNE 1993, FIGURE 1B.	8-10, 12, 17, 18
Y	US 5,177,669 A (JUSKEY et al) 05 JANUARY 1993, FIGURE 6.	8-10, 12, 17, 18
A	JP 4-99056 A (HASHIMOTO) 31 MARCH 1992, FIGURES 2, 3.	1-22



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:	"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
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Date of the actual completion of the international search

13 APRIL 1997

Date of mailing of the international search report

21 APR 1997

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